REMARKS

In the Office Action[1], the Examiner took the following actions:

> objected to claims 4, 5, and 15 due to informalities;
>
> rejected claims 1-3 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,498,891 to Sato; and
>
> indicated that claims 4-15 were drawn to allowable subject matter and would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims.

Applicants thank the Examiner for the indication of allowable subject matter, but respectfully traverse the rejection.

Applicants have amended claims 1, 2, 4-11, and 13-15, and added new claim 21. Claims 16-20 are canceled without prejudice or disclaimer of their subject matter. Upon entry of this amendment, claims 1-15 and 21 remain pending and under current examination.

Specifically, Applicants have:

> amended claim 1 to recite a "double gate structure comprising top and bottom gate electrodes, the bottom gate electrode being located at a lower level than the main surface." Similarly, claim 2 has been amended to recite that a "bottom gate electrode is provided in the semiconductor substrate, a part of the side of the main surface of the semiconductor substrate is placed between the top gate electrode and bottom gate electrode." Support for the amendments to claims 1 and 2 can be found, for example, in FIG. 8B and its corresponding description in Applicants' specification, including polysilicon film 9.

[1] The Office Action contains a number of statements reflecting characterizations of the related art and the claims. Regardless of whether any such statement is identified herein, Applicants decline to automatically subscribe to any statement or characterization in the Office Action.

Claims 4, 5, and 15 have been amended in a manner consistent with the Examiner's comments at page 2 of the Office Action. Claim 4 has also been rewritten in independent form and incorporates subject matter recited in independent claims 1, 2, and 3.

Claims 6-11 have been amended to correct improve readability. Claim 6 has also been amended to be consistent with amended claims 4 and 5. Claims 8-11 have also been amended to correct a minor typographical error.

Claims 13 and 14 have been amended to be consistent with amended claims 4, 5, and 15. Claim 13 has also been amended to improve readability.

New claim 21 recites that "the region having the deeper bottom is located under the top gate electrode." Support for new claim 21 can be found, for example, in FIG. 8C and its corresponding description in the specification including region T in silicon oxide film 7.

Accordingly, Applicants deem the objection to claims 4, 5, and 15 overcome. Applicants respectfully request that the Examiner withdraw the objection to claims 4, 5, and 15.

Applicants respectfully traverse the rejection of claims 1-3 under 35 U.S.C. § 102(b) as being anticipated by Sato. In order to support a rejection under 35 U.S.C. § 102, each and every element of each claim in issue must be found, either expressly described or under principles of inherency, in that single reference. Furthermore, "[t]he identical invention must be shown in as complete detail as is contained in the ... claim." *See* M.P.E.P. § 2131, quoting *Richardson v. Suzuki Motor Co.*, 868 F.2d 1126, 1236, 9 U.S.P.Q. 2d 1913, 1920 (Fed. Cir. 1989).

Claim 1 recites "a semiconductor substrate including a main surface . . . [and a] double gate structure comprising top and bottom gate electrodes, the bottom gate electrode being located at a lower level than the main surface." In contrast, FIG. 6 of

Sato discloses a floating gate 3 and a word line or control gate 5 formed on insulating layers 2 and 8. FIG. 6 also illustrates that insulating layers 2 and 8 are formed on or in substrate 1 and source region 9. However, FIG. 6 of Sato teaches that floating gate 3 and word line or control gate 5 formed on insulating layers 2 and 8 are above substrate 1 and any corresponding "main surface" thereof. Thus, to the extent that the Examiner may be construing floating gate 3 and control gate 5 as corresponding to the claimed "top and bottom gate electrodes," Sato still fails to teach or suggest a "bottom gate electrode being located at a lower level than the main surface" of a semiconductor substrate as recited in claim 1.

Sato therefore does not anticipate claim 1 at least because the reference fails to disclose each and every element recited in claim 1. Claims 2 and 3 depend from claim 1 and are not anticipated by Sato for at least the same reasons as independent claim 1. Accordingly, Applicants respectfully request that the Examiner reconsider and withdraw the rejection of claims 1-3 based on Sato.

Furthermore, new claim 21 depends from claim 1, and is allowable over Sato at least due to its dependence from base claim 1. Claim 4 has been rewritten in independent form and also amended to overcome the Examiner's objections discussed above. Accordingly, claim 4 is in condition for allowance. Claims 5-15 depend from independent claim 4 and are allowable at least due to their dependence from claim 4.

In view of the foregoing amendments and remarks, Applicants respectfully submit that the pending claims are in condition for allowance. Applicants respectfully request prompt and favorable action by the Examiner and allowance of claims 1-15 and 21.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

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